Monolithic Quantum Tunnel Diode-Based C-Band Oscillator and LNA

J. I. Bergman, S. Han[†], J. Laskar, N. El-Zein[1], S. Ageno[1], M. Deshpande[1], and V. Nair[1]

Microelectronics Research Center
Department of Electrical and Computer Engineering, Georgia Institute of Technology
791 Atlantic Drive NW, Atlanta, GA 30332-0269, USA

[1]Motorola Labs, Motorola, Inc.
7700 S. River Parkway, Tempe, AZ 85284, USA

[†]now with RF Solutions
2100 West Peachtree Street, Atlanta, GA 30309

***Abstract* – We report on the design and microwave performance of a novel tunnel diode-based oscillator designed for 5 GHz in a monolithic IC technology. The fundamental output power of the oscillator is –18.8 dBm at 4.7 GHz, with second and third harmonic power levels at –43.2 dBm and –40.5 dBm, respectively. Phase noise of –87.0 dBc/Hz at 1 MHz was observed. While output power can be greatly increased by combining the tunnel diode with an integrated transistor, this design offers excellent compactness and low power consumption. In addition, an LNA design for 6 GHz in the same IC technology is presented.**

I. INTRODUCTION

Semiconductor devices that exhibit negative differential resistance (NDR) have been an area of great interest for future application in high-speed, high-density integrated circuits. To date, novel digital circuits have been developed which take advantage of the NDR characteristic to enable greater functionality when compared to conventional transistor-only integrated circuits. Examples include digital logic [1,2], and low-power, high-density memory cells operating at room temperature [3]. High-speed analog circuits have also been demonstrated, such as a 4-bit, 2-Gsps flash analog-to-digital converter, implemented in a monolithic HFET-resonant tunneling diode (RTD) technology [4], with the potential to yield 20 Gbps comparators. While most of the research effort into integrated NDR circuits has been focused on digital circuits, NDR devices have great potential to improve the speed and functional density of microwave integrated circuits as well.

While most monolithic NDR-transistor processes have integrated intraband RTDs with either HFETs or heterojunction bipolar transistors (HBTs), heterostructure interband tunneling diodes (HITDs) hold promise, especially in microwave analog circuits. Although RTDs can offer high peak-current densities and peak-to-valley current ratios (PVCR), the HITD offers a high PVCR combined with a larger voltage range over which the diode operates in the NDR region, properties which are useful in microwave applications. A MMIC technology that includes HITDs along with transistors as active devices offers the promise of better performing oscillators, mixers, and low-noise amplifiers (LNA).

Combined HITD-HFET (HITFET) devices have been employed to yield highly compact oscillators, due to the ability to merge some of the passive components required in a conventional oscillator into the HITFET. A HITFET-based X-band voltage-controlled oscillator (VCO) with a dual series-connected HITD was fabricated exhibiting 4.23 dBm of output power at a frequency of 8.2 GHz, with a tuning range of up to 60 MHz [5]. In this paper, we report a novel HITD-only oscillator designed for 5 GHz operation that offers high circuit density and very low power consumption.

In addition to oscillators, HITDs offer potential for microwave LNAs by virtue of the low noise quantum electronic devices offer while providing gain. Designs show that an LNA with an ultra-low noise 3-5 dB gain HITD-based amplifier as the first stage can offer similar gain as an HFET-only design with the overall noise figure limited by that of the HITD amplifier.

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II. QMMIC TECHNOLOGY

The oscillator and LNA reported were fabricated by Motorola Research Labs' QMMIC (quantum MMIC) process. The baseline process incorporates vertically integrated HFETs and HITDs which are grown by molecular beam epitaxy (MBE) on InP substrates [6]. The InAlAs/InGaAs-based HEMTs are fabricated with gate lengths of 0.8-μm, and exhibit f_T of 20 GHz. The HFETs can be scaled to improve gain and achieve higher frequency operation.

The monolithic process allows for flexibility in meeting the range of matching and power conditions for microwave circuit design by varying the doping profiles and quantum well widths to produce optimal HITD characteristics for the application of interest. For the circuits detailed in this paper, mixed Esaki HITDs were employed, which yielded a high peak current density of 40 kA/cm^2 and a good PVCR of 8. While higher peak-to-valley ratios are achievable with InGaAs/InAlAs HITDs, it is compromised in order to yield a higher peak current density, which is more important in analog microwave applications because significant current span is needed in the NDR region.

After the active devices and epitaxial resistors are fabricated, the process is completed with MIM capacitors, spiral inductors, and two metallization layers. No backside processing is performed, and conventional compound semiconductor fabrication methods are utilized throughout.

III. DESIGN AND CHARACTERIZATION

In designing the 5 GHz oscillator and LNA, accurate modeling of the HITD and HFET is essential. For the HFET small-signal model, a linear hybrid-π model was used with parameters fitted from s-parameter data measured up to 10 GHz. To accurately model the HITD, an equation-based model was developed using DC measurements to measure the device's nonlinearity, and s-parameter measurements up to 10 GHz to determine the reactive components. The complete HITD model is shown in Figure 1, with the equation based voltage-controlled current source containing the diode's nonlinear I-V characteristics.

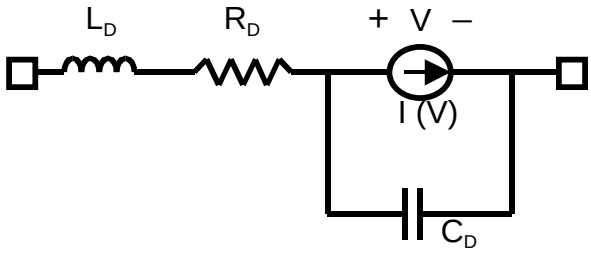

Fig. 1. Circuit model of an HITD as used in circuit simulations. The nonlinear voltage-controlled current source is based on a fifth-order polynomial.

The current source is governed by the polynomial:

$$I(V) = a_1 V + a_2 V^2 + a_3 V^3 + a_4 V^4 + a_5 V^5 \quad (1)$$

where the coefficients a_1, a_2, …, a_5 are determined by parameter extraction from device measurements. The model parameters for a 2.5-μm^2 HITD are summarized in Table 1.

TABLE I
HITD MODEL PARAMETERS

Parameter	Value
L_D	0.2 nH
C_D	83 fF
R_D	12 Ω
a_1	0.02542
a_2	–0.1905
a_3	0.5591
a_4	–0.7423
a_5	0.372

Using this HITD model, the 5 GHz HITD oscillator was designed, as shown in Figure 2. The oscillator has only one power supply, the diode bias, and is designed for a 50-ohm load. Since there are no HFETs in the design, the active device area is very small, so that nearly all layout area is occupied by the passives, as can be seen in Figure 3. Due to the single HITD design, the output power is expected to be low, but likewise the circuit power consumption will be proportionately low. For increased output power, HITD can be combined with an HFET.

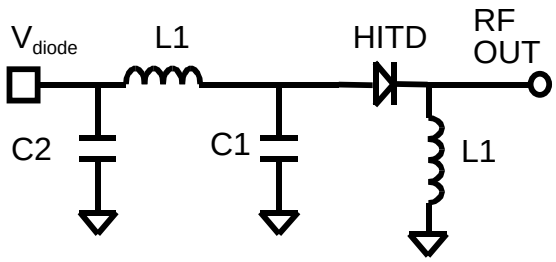

Fig. 2. Circuit schematic of the 5 GHz HITD oscillator. The bias voltage is 0.45 volts, corresponding to the peak negative differential conductance of the HITD.

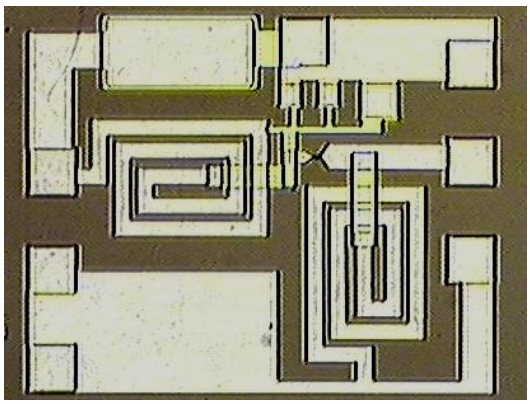

Fig. 3. Photomicrograph of the fabricated 5 GHz HITD oscillator. Dimensions are 500 × 650 μm.

The oscillator was characterized using an Agilent 8565E RF spectrum analyzer. On-wafer probing was employed to minimize external parasitics due to bonding; the DC bias was applied using DC probes with bypass capacitors connected between the power and ground needles, yielding a probe inductance of about 0.5 nH. The DC bias was applied at 0.45 volts, at the HITD's peak negative differential conductance. The output was probed using 150-μm pitch ACP40 ground-signal-ground RF probes from Cascade Microtech.

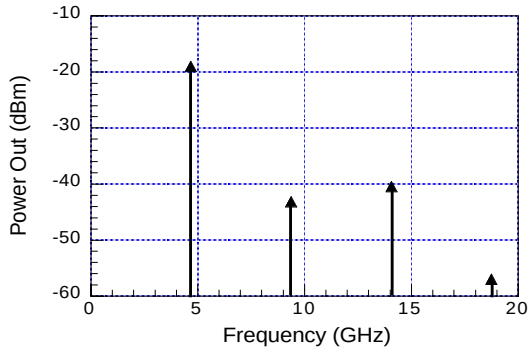

Fig. 4a. Output spectrum of the HITD oscillator showing harmonics.

The measured oscillator output spectrum is shown in Fig. 4a. The fundamental output power is –18.83 dBm at 4.70 GHz. The second, third, and fourth harmonic output levels are –43.2, -40.5, and –57.0 dBm, respectively. The frequency spectrum of the oscillator is shown in Figure 4b. The phase noise was measured to be –87.0 dBc/Hz at 1 MHz from the peak. The total power consumption is 0.32 mW.

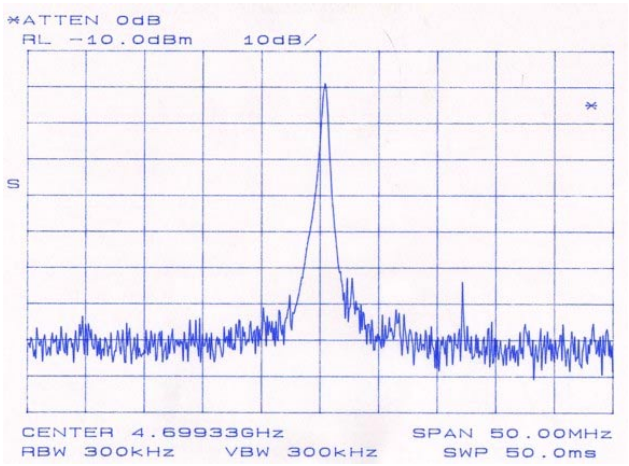

Fig 4b. Frequency spectrum of the HITD-based oscillator. (Center frequency is 4.70 GHz, the amplitude is –18.83 dBm, and the span is 50 MHz.)

The circuit schematic for the 6 GHz LNA is shown in Figure 5, with the layout illustrated in Figure 6. The LNA consists of two stages. The first is an HITD amplifier consisting of a 5 × 2.5 μm^2 HITD with an inductor that serves as both the RF block and an impedance matching element. The second stage is a FET-based LNA designed for a 50-ohm load. The combined LNA offers potential for lower noise figure than a FET-only based design in the same MMIC technology.

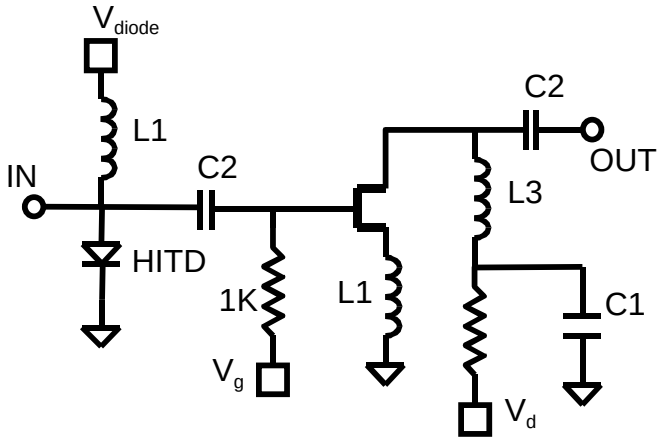

Fig. 5. Circuit schematic of 6 GHz LNA. Values for bias voltages are V_{diode} = 0.45V, V_g = -1.0V, and V_d = 1.0V.

While the first stage provides only about 3 dB of gain, it offers a lower noise figure than the second HFET stage, resulting in a lower noise figure than a FET-only based design in the same MMIC technology. Simulations estimate a gain of 6 dB and a noise figure of 2 dB with a 50-ohm source impedance.

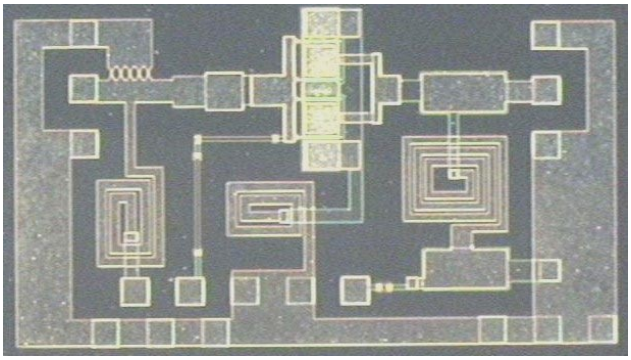

Fig. 6. Photograph of the 6 GHz HITD-HFET LNA.

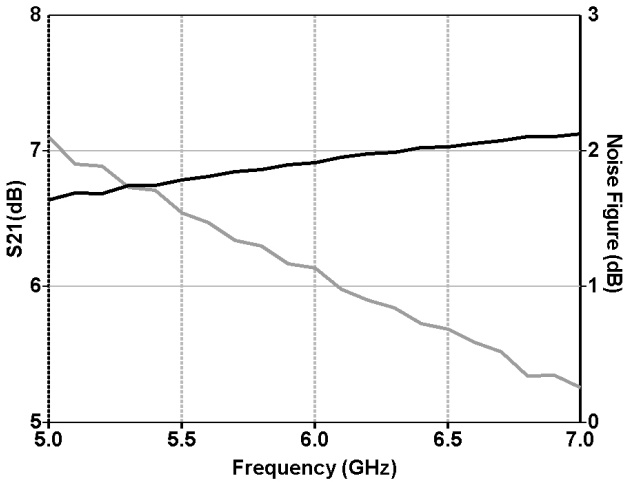

Fig. 7. Simulated LNA performance. Gain is indicated in gray, while noise figure with 50-ohm impedance is shown in black.

IV. Conclusion

In summary, a novel design for a low-power oscillator has been demonstrated. This design takes advantage of an integrated circuit technology that allows for the monolithic co-integration of NDR HITDs with conventional high-frequency HFETs and passives. Using measurement derived device models, RF circuit designs can be realized with very good correlation to simulation. In addition to oscillators, HITD-HFET based designs have potential to yield LNAs with superior performance relative to their HFET-only counterparts in the same FET technology.

V. References

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